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Hardware Equivalence Checking Problems Submitted to the SAT Competition 2024

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Abstract—We describe our benchmarks submitted to the SAT competition 2024 encoding hard isomorphic combinational equivalence checking problems of benchmarks from the hardware model checking competition 2012, 2017 and 2020.

Our pre- and inprocessing technique "clausal congruence closure" [1] is inspired by classical congruence closure [2], a key procedure in SMT solvers [3]. It extracts Tseitin encoded AND, ITE and XOR gates from a CNF, and then hashes their right-hand-side to find matching left-hand-side literals. These are then set to be equivalent using a union-find data-structure. Gates containing matched literals are rewritten and rehashed to find further equivalences. This process continues until no more unprocessed equivalences are left and is interleaved with unit-propagation in case rewriting produces new unit literals.

Clausal congruence closure can identify isomorphic subcircuits of Tseitin encoded circuits if only the CNF is given. In order to show-case the effectiveness of our approach, we generated equivalence checking problems, which compare two identical copies of a given circuit. Such equivalence checking problems of isomorphic circuits (we also call them isomorphic miters) are solved instantly by our approach, while pure state-of-the-art CDCL solvers have a hard time. Their decision heuristics fail to find the short resolution proofs produced by clausal congruence closure.

We generated such isomorphic miters from circuits used in the Hardware Model Checking Competition (HWMCC) 2012 [4], 2017 [5], and 2020 [6], by simply interpreting the state elements (flip-flops/latches) as additional inputs and checking equivalence of output and next-state functions. Compared to a similar benchmark set submitted to the SAT Competition 2013 [7], which also used the 2012 HWMCC circuits, we employ a more sophisticated Tseitin encoding [1]. The 2020 benchmarks are also used in [8].

As in [7], each pair of isomorphic circuits is given as and-inverter graph (AIG) in the AIGER format [9] but instead of directly encoding each AND separately we try to match binary AND gates to binary XOR and ITE gates. If successful we use a more compact CNF encoding for the XOR and ITE gates instead. This optimized encoding can reduce the size of the resulting CNF substantially and also in our experience produces easier to solve benchmarks.

After producing 975 isomorphic miters for 341 HWMCC'12 benchmarks, 300 from HWMCC'17 and 334 from HWMCC'20, we tried to solve them with the newest version of Kissat with and without clausal congruence closure. This gave exactly 24 CNFs (3 from HWMCC'12, 6 from HWMCC'17, 25 from HWMCC'20) for which the version without congruence closure took more than 2500 seconds (on a machine roughly twice as fast as the StarExec nodes) while easy for clausal congruence closure.

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